

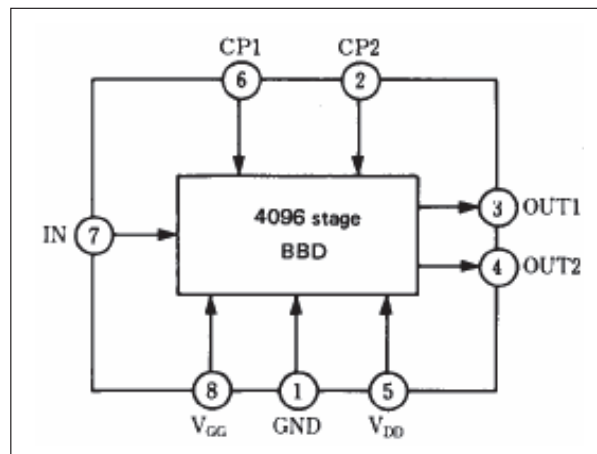
1. Description

The V3205 is a 4096-stage low-noise, low-voltage BBD analog delay line that provides analog signal delays of up to 204.8 ms and is particularly suitable for the generation of sound effects (reverb, echo, phaser, flanger, etc.) in audio equipment such as karaoke microphones, guitar effects pedals, etc.

2. Features

- **Variable Delay of Audio Signals: 20.48 ms ~ 204.8 ms**
- **Wide Supply Voltage: 4 ~ 9 V**
- **Wide Dynamic Range: S/N = 67 dB typ.**
- **Package outline: Special DIL-8 (V3205D)**
- **ROHS compliant (PB-free)**

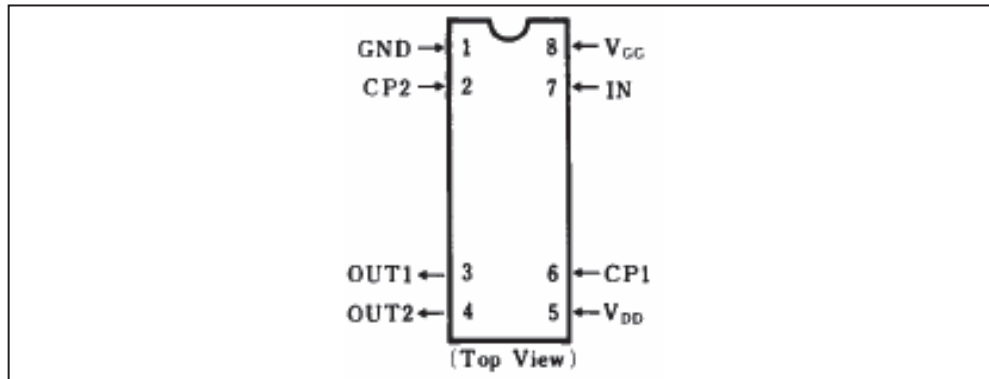
3. Block Diagram



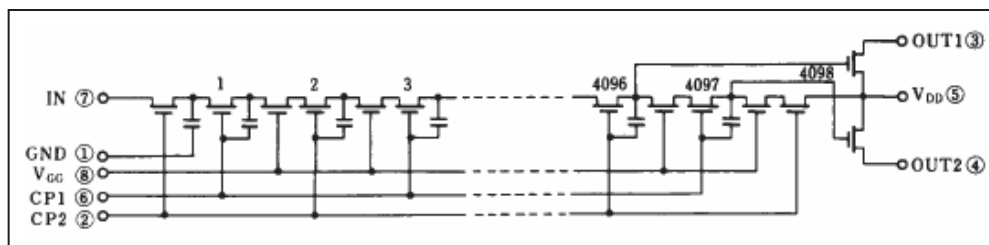
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Rev. 1.0

4. Pin Configuration



5. Circuit Diagram



6. Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	+5, 14/15 V_{DD}	V
Signal Delay Time	t_D	20.48 ~ 204.8	ms
Total Harmonic Distortion	THD	0.8	%
Signal to Noise Ratio	S/N	67	dB

7. Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Terminal Voltage	$V_{DD}, V_{GG}, V_{CP}, V_i$	-0.3 ~ +11	V
Output Voltage	V_O	-0.3 ~ +11	V
Operation Ambient Temp.	T_{opr}	-20 ~ +60	°C
Storage Temp.	T_{stg}	-55 ~ +125	°C

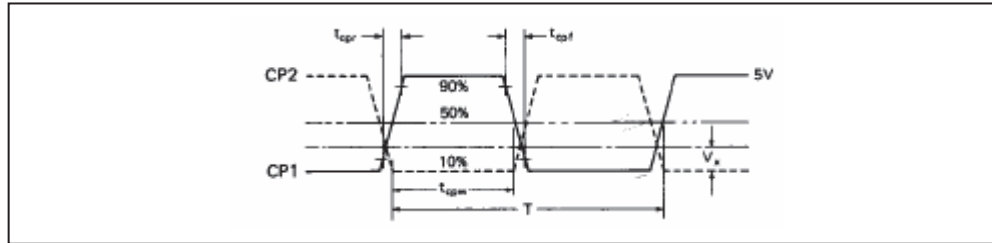
8. Operating Conditions (Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
Drain Supply Voltage	V_{DD}		+4	+5	+9	V
Gate Supply Voltage	V_{GG}			$14/15 V_{DD}$		V
Clock Voltage High	V_{CPH}			V_{DD}		V
Clock Voltage Low	V_{CPL}		0		+0.5	V
Clock frequency	f_{CP}		10		100	KHz
Clock Pulse Width *1	t_{CPW}				$0.5T^*2$	
Clock Rise Time *1	t_{CPR}				500	ns
Clock fall Time *1	t_{CPF}				500	ns
Clock Input Capacitance	C_{CP}				2800	pF
Clock Cross Point	V_X		0		$0.3V_{CPH}$	V

9. Electrical Characteristics (Ta = 25°C, VDD = VCPH = 5V, VCPL = 0V, VGG = 14/15 VDD, RL=100k)

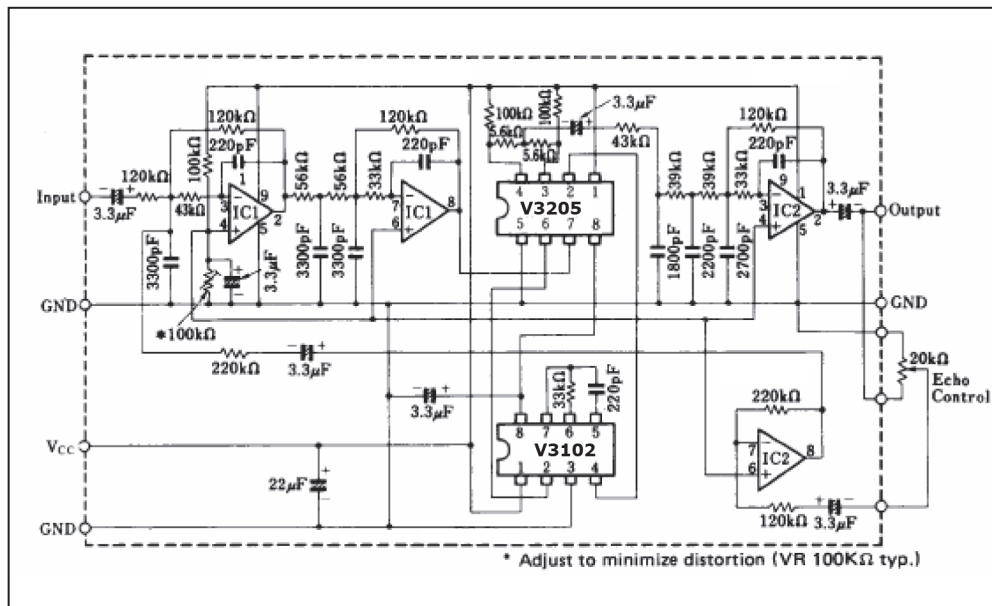
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Signal Delay Time	t_O		20.48		204.8	ms
Input Signal Frequency	f_i	$f_{CP} = 40\text{kHz}$, Output Attenuation $\leq 3\text{dB}$	6			kHz
Input Signal Swing	V_i	THD = 2.5%	0.36			V_{rms}
Insertion Loss	L_i	$f_{CP} = 40\text{kHz}$, $f_i = 1\text{kHz}$	-4	0	4	dB
Total Harmonic Distortion	THD	$f_{CP} = 40\text{kHz}$, $f_i = 1\text{kHz}$, $V_i = 0.25 V_{rms}$		0.8	2.5	%
Output Noise Voltage	V_{ON}	$t_{CP} = 100\text{kHz}$, Weighted by "A" curve			0.35	mV_{rms}
Signal to Noise Ratio	S/N			67		dB

* 1 Clock Pulse Waveform



*2 $T = 1/f_{CP}$ (Clock Period)

10. Application Circuit



11. Mechanical Specifications

